ANALOG DEVICES

AN-749 APPLICATION NOTE

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Configuration Examples for the ADAV801 and ADAV803

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INTRODUCTION

The AN-749 Application Note describes the steps involved in setting up the ADAV80x DVD-recordable codec for the configurations that are used most often. This application note should be used in conjunction with the appropriate data sheet. ADAV80x refers to the ADI ADAV801 codec and the ADI ADAV803 codec.

EXAMPLE 1

ADC Sampling at 48 kHz with MCLKI = 12.288 MHz

In this example, it is assumed that the user wants to configure the ADAV80x to have the ADC sampling at 48 kHz when a 12.288 MHz clock is available at the MCLKI pin. The ADC digital data is to be made available on the record port. Since the default sample rate of the ADC is MCLK/256, the MCLKI frequency of 12.288 MHz will provide a sample rate of 48 kHz.

As shown in Figure 1, the MCLK for the ADC can be selected by programming Bit 4, Bit 3, and Bit 2 of the Internal Clocking Control Register 1. The ACLK bits in this register should be programmed with 0b001 to select MCLKI as the clock source. The internal clock ICLK2 can also be programmed at this stage to be equal to MCLKI. The register is therefore programmed with 0bxxx00101. To ensure that the record output port is operating at the same speed as the ADC, the clock for the port should be the same as for the ADC. The record port has a choice of three clock options: ICLK1, ICLK2, or PLL clock; it can also be set as a slave. As shown in Figure 1, either ICLK1 or ICLK2 can be configured to be equal to MCLKI by programming the appropriate bits in the internal clocking control registers. When the record port clock source is selected with ICLK1 or ICLK2, as appropriate the port will act as a master and the OLRCLK and OBCLK pins will be outputs. This example will use ICLK2. The serial word length and serial data format can be selected by programming the appropriate bits in the record port control register. The Datapath Control Register 1 should be programmed such that the ADC is the selected source for the record port by setting the REC2-0 bits to 0b000.

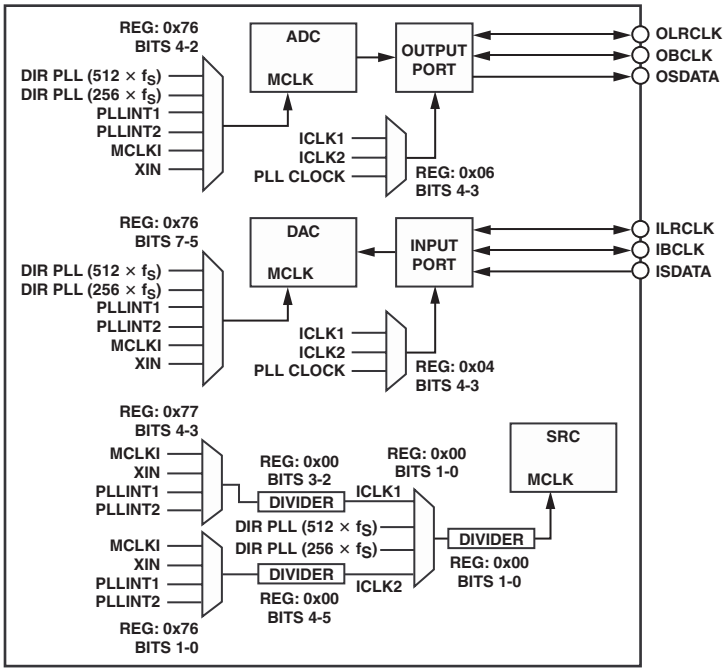

Figure 1. ADAV80x Clocking Scheme

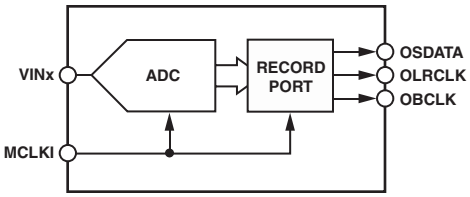

Figure 2. Using the ADC with MCLKI

EXAMPLE 2
ADC Sampling at 44.1 kHz Using the PLL

This example requires that the PLL be used to generate a suitable system clock such that the ADC can sample an input signal at 44.1 kHz. As with the previous example, the ADC requires an MCLK that is 256 times the required sample rate. It is assumed that the PLL oscillator is driven by a 27.000 MHz crystal connected between the XIN and XOUT pins. The crystal oscillator is enabled by clearing the XTLPD bit in PLL Control Register 1. The PLLs are enabled by clearing the appropriate PLLxPD bit in the same register, i.e., by writing 0b00x0000x to PLL Control Register 1. The MCLK required by the ADC will be 256 $\times$ 44100 = 11.2829 MHz. This can be selected by setting the FSx bits to 44.1 kHz and SELx to 256 in PLL Control Register 2. Where PLL1 is to be used, writing 0bxxxx1100 to the register is required.

As in the previous example the clock for the record output port should be the same as the ADC MCLK. The ICLK1 or ICLK2 should therefore be selected to be either PLLINT1 or PLLINT2, depending on the PLL being used. The Datapath Control Register 1 should be programmed such that the ADC is the selected source for the record port by setting the REC2-0 bits to 0b000. Figure 3 shows how the ADAV80x is configured.

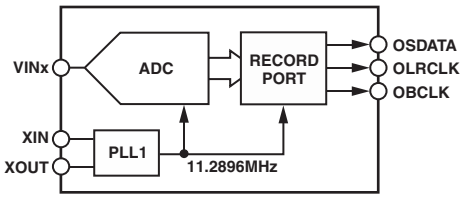

Figure 3. Using the ADC with the PLL

EXAMPLE 3
DAC Running at 48 kHz

In this example the digital data for the DAC is provided via the playback port. This port operates as a slave with an external audio controller providing the ILRCLK, IBCLK, and ISDATA. The DAC requires that the data be provided at a rate equal to the DAC MCLK/256. It is therefore assumed that the external audio controller is providing a suitable audio clock to the XIN pin. The DAC MCLK should be set to XIN by setting the DCLK bits to 0b000 in the Internal Clocking Control Register 1, i.e., by writing 0b000xxxxx. The Datapath Control Register 2 should be programmed such that the playback port is the selected source for the DAC by setting the DAC2-0 bits to 0b010 giving 0b00010xxx. Since the playback port is a slave by default and clocked externally by the audio controller, there is no need to select a clock for the port as was the case in the previous two examples. Note that the DAC is muted by default and should be unmuted before the output signal will be present on the VOUT pins.

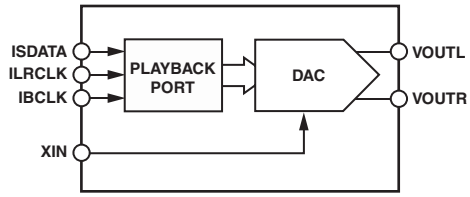

Figure 4. DAC Configuration

EXAMPLE 4
Running the DAC from the DIRIN

This example demonstrates how to configure the ADAV80x so that an SPDIF stream applied to the DIRIN pin can be used as an audio source for the DAC.

The first step is to set the DAC source as the SPDIF receiver (DIR). This is done by programming the Datapath Control 2 Register with 0bxx001xxx. The clock source for the DAC then needs to be set as the SPDIF recovered clock, which is 256 $\times$ f_S, by writing 0b101xxxxx to the Internal Clocking Control 1 Register. The threshold level of the DIRIN pin should be set to the appropriate level depending on whether the SPDIF source is operating at digital logic levels or according to the IEC60958-3 standard. This can be achieved by setting or clearing Bit 4 of the PLL output enable register. The DACs are muted by default and must be unmuted for normal operation. This is done by writing 0bxxxxxx00 to the DAC Control 1 Register.

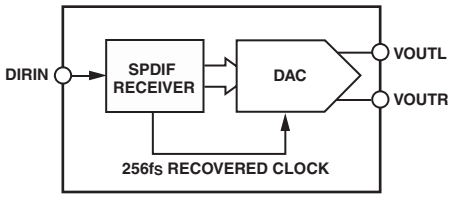

Figure 5. DAC Configuration Using DIRIN

EXAMPLE 5
Using the Sample Rate Converter

This example will take data supplied on the playback port at 44.1 kHz, pass it through the sample rate converter (SRC), and send it to the record port at a rate of 48 kHz. It is assumed that whichever data source is providing the playback port with data is also providing a 256 $\times$ f_S clock to the MCLKI pin.

The sample rate at the output of the SRC is determined by clocking the port at the desired rate. In order to achieve this, the record port is set as a master and supplied with a clock that is 256 times the required sample

rate. For a sample rate of 48 kHz, the required clock rate is 12.288 MHz. The PLL will be used to generate the clock. To set up the required sources for the SRC and record port, it is necessary to write 0b10100xxx to the Datapath Control Register 1.

For this example PLL1 will be used as the clock source for the record port. To achieve the correct clock frequency, the PLL should be programmed for 48 kHz, 256 × f_S, with clock doubling disabled. The PLL Control 2 Register should, therefore, be programmed with 0bxxxx0000. The PLL and XTAL oscillator must also be enabled by programming PLL Control 1 Register with 0b0000x00x.

The internal clocking control registers need to be set up with the appropriate clocks for the record port and SRC master clock. In this example, ICLK2 will be used for the record port and ICLK1 will be used as the SRC master clock. The Internal Clocking Control 1 Register should be programmed with 0bxxxxxx10 (for ICLK2), and Internal Clocking Control 2 Register should be programmed with 0b00010xx0. The final step is to unmute the SRC by writing 0b0xxxxxxx to the SRC group delay and mute register.

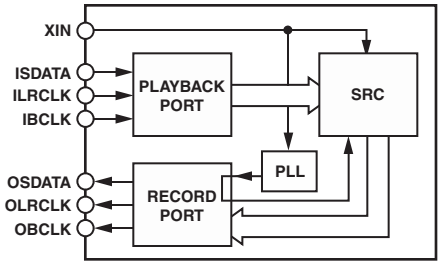

Figure 6. Using the SRC

EXAMPLE 6

Using the SPDIF Transmitter to Transmit ADC Data

This example describes how to use the integrated SPDIF transmitter to transmit data received from the ADC. Setting up the ADC is similar to Example 6. The ADC is set up to use a PLL to clock the ADC. The same PLL clock is used as either ICLK1 or ICLK2. The Datapath Control 2 Register is programmed with 0b00xxx000 to select the ADC as a source. The SPDIF transmitter control register should be programmed with 0b0xxxx001 (for ICLK1) or 0b0xxxx011 (for ICLK2) to select the clocking source and enable the transmitter.

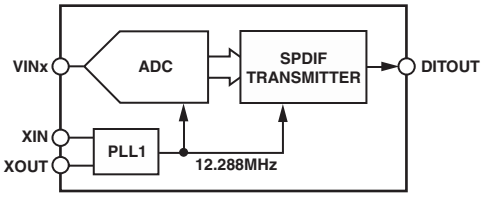

Figure 7. ADC Configuration Using DITOUT

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